In the claims:

1. (Currently Amended) An apparatus, comprising:

a queue;

~~an~~ a programmable event ~~selection~~ conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not empty signal from the queue; and

a counter to increment in response to an increment event signal delivered by the event selection logic unit, the counter to decrement in response to a decrement event signal delivered by the event selection logic unit.

2. (Currently Amended) The apparatus of claim 1, the event ~~selection~~ conditioning logic unit to further receive an inverted version of the queue not empty signal.

3. (Original) The apparatus of claim 2, further comprising a data register coupled to the counter.

4. (Currently Amended) The apparatus of claim 3, further comprising a comparator including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the counter, and the output provided to the event ~~selection~~ conditioning logic unit.

5. (Currently Amended) The apparatus of claim 4, the event ~~selection~~ conditioning logic including programmable functions to allow a variety of

combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events.

6. (Original) The apparatus of claim 5, further comprising a block of registers including a command register and a status register.

7. (Currently Amended) An apparatus, comprising:

a queue;

~~an~~ a programmable event ~~selection~~ conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not empty signal from the queue; and

a first counter to increment in response to a first increment event signal delivered by the event selection logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event selection logic unit; and

a second counter to increment in response to a second increment event signal delivered by the event selection logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event selection logic unit.

8. (Currently Amended) The apparatus of claim 7, the event ~~selection~~ conditioning logic unit to further receive an inverted version of the queue not empty signal.

9. (Original) The apparatus of claim 8, further comprising a data register coupled to the first counter.

10. (Currently Amended) The apparatus of claim 9, further comprising a comparator including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the first counter, and the output provided to the event ~~selection~~ conditioning logic unit.

11. (Currently Amended) The apparatus of claim 10, the event ~~selection~~ conditioning logic including programmable functions to allow a variety of combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events.

12. (Original) The apparatus of claim 11, the second counter to increment in response to the comparator output indicating that the first counter value matches the data register value.

13. (Original) The apparatus of claim 12, further comprising a block of registers including a command register and a status register.

14. (Currently Amended) A system, comprising:

a processor; and

a system logic device coupled to the processor, the system logic device including

a queue,

~~an~~ a programmable event ~~selection~~ conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not empty signal from the queue, and

a counter to increment in response to an increment event signal delivered by the event selection logic unit, the counter to decrement in response to a decrement event signal delivered by the event selection logic unit.

15. (Currently Amended) The system of claim 14, the event ~~selection~~ conditioning logic unit to further receive an inverted version of the queue not empty signal.

16. (Original) The system of claim 15, further comprising a data register coupled to the counter.

17. (Currently Amended) The system of claim 16, the system logic device further including a comparator including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the counter, and the output provided to the event ~~selection~~ conditioning logic unit.

18. (Currently Amended) The system of claim 17, the event ~~selection~~ conditioning logic including programmable functions to allow a variety of combinations of the queue enter, queue exit, queue not empty, queue empty, and comparator output signals to serve as increment or decrement events.

19. (Original) The system of claim 18, the system logic device further including a block of registers including a command register and a status register.

20. (Currently Amended) A method, comprising:

delivering a queue enter signal, a queue exit signal, and a queue not empty signal to ~~an~~ a programmable event ~~selection~~ conditioning logic unit;

asserting an increment event signal in response to an occurrence of a first programmable combination of the queue enter signal, the queue exit signal, and the queue not empty signal;

incrementing a counter in response to the assertion of the increment event signal;

asserting a decrement event signal in response to an occurrence of a second programmable combination of the queue enter signal, the queue exit signal, and the queue not empty signal; and

decrementing the counter in response to the assertion of the decrement event signal.

21. (Original) The method of claim 20, further comprising storing the counter value in a data register.

22. (Original) The method of claim 20, further comprising comparing the counter value with a data register value.